Developments In DDR Main Memory Platform Design

February 15, 2001

Agenda

- DDR standard update
- DDR systems implementations today
- Improving DDR channel bandwidth
- Migrating to DDR333/PC2700

DDR Standard Update

The DDR Standard

- All standards are in place
  - Components and modules
- There have been a few minor tweaks
  - Addition of four new SPD bits to better define module performance capability
- On-line access to the latest data
  - JEDEC Web site
  - Micron Design Toolbox at http://reg.muscp.com/mk/get/TOOLBOXREG

DDR SPD

- Byte 41 added to define $^{t}RC_{min}$
  - Have been using Byte 27 ($^{t}RP_{min}$) + Byte 30 ($^{t}RAS_{min}$)
  - $^{t}RP_{min}$ + $^{t}RAS_{min}$ do not always equal $^{t}RC_{min}$
  - $^{t}RC_{min}$ must be defined by using Byte 41
- Byte 42 added to define $^{t}RFC_{min}$
  - Refresh cycle rate use READ/WRITE cycle rate $^{t}RC_{min}$
  - $^{t}RFC_{min}$ is one or two clocks longer than $^{t}RC_{min}$
  - Refresh cycle rate must use refresh cycle rate - $^{t}RFC_{min}$

DDR SPD

- Byte 22 supports two new optional features
  - Bit 6 defines Concurrent Autoprecharge (AP) support
    - 1 indicates support for optional feature
    - 0 indicates no support for optional feature
  - Bit 7 defines RAS lockout support
    - Applies only when AP is enabled
      - ^{t}RCD is replaced by ^{t}RAP when AP is enabled
    - 1 indicates support for optional feature
      - $^{t}RAP_{min} = {}^{t}RCD_{min}$
    - 0 indicates no support for optional feature
      - $^{t}RAP_{min} = {}^{t}RAS_{min} - {}^{t}CK$ * (Burst Length divide by 2)

Today’s DDR designs

PC1600/2100 DDR Design Assumptions

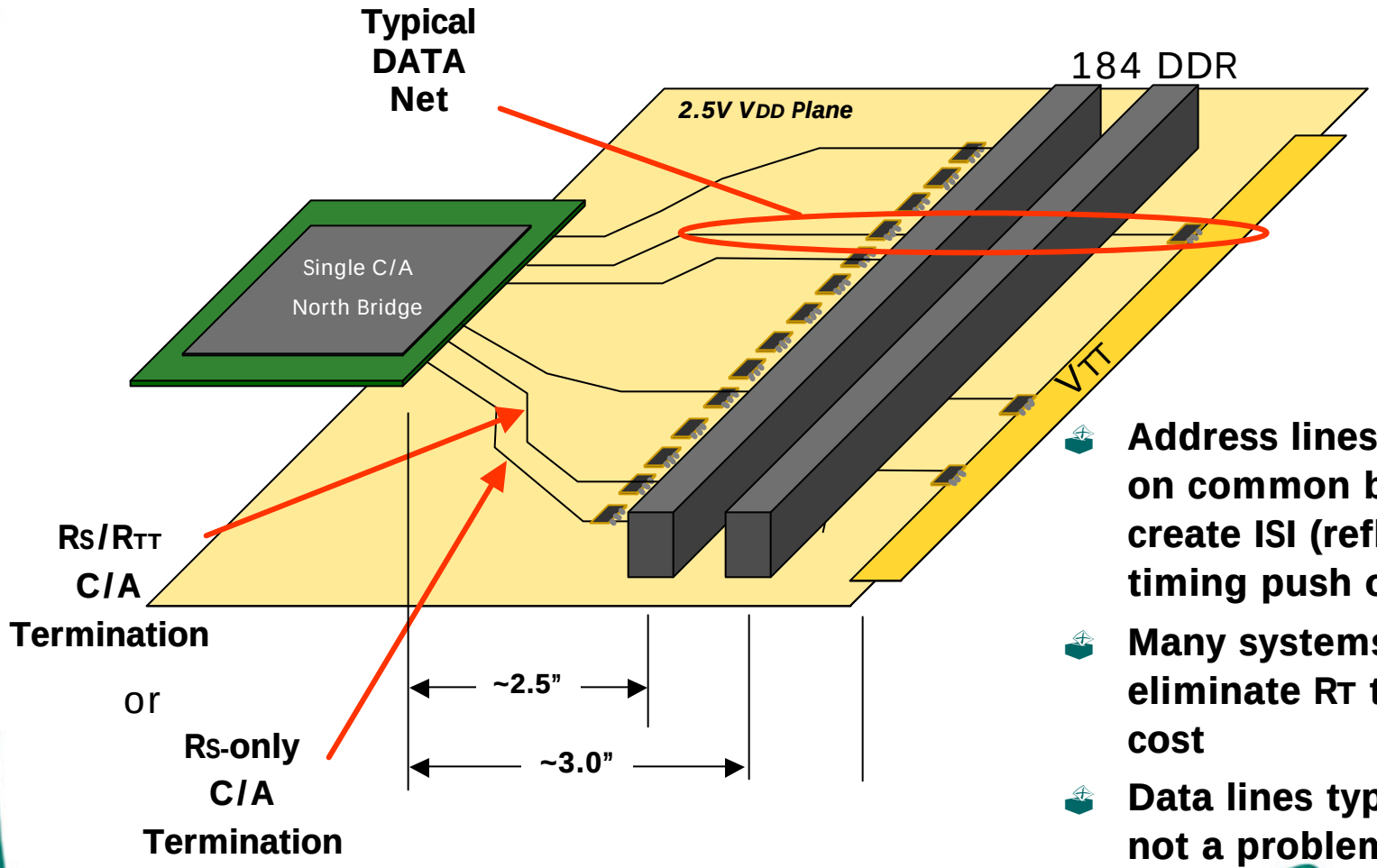
- Module designs assumed DDR—only memory systems
- Mixed SDR/DDR systems exist for cost/availability hedge today
  - Give many an opportunity to assess new technology in the second generation designs
  - Opportunities to assess cost reduction or higher performance options

Desktop

- **Motherboards taking many forms**
  - **DDR cost and availability has generated mixed SDR - DDR systems**
    - **The standard has not included this kind of design**
    - **Recommend caution; thoroughly test such systems**
    - **These designs push the design parameters of DDR and PC133 SDR**

Example of Pure DDR Channel

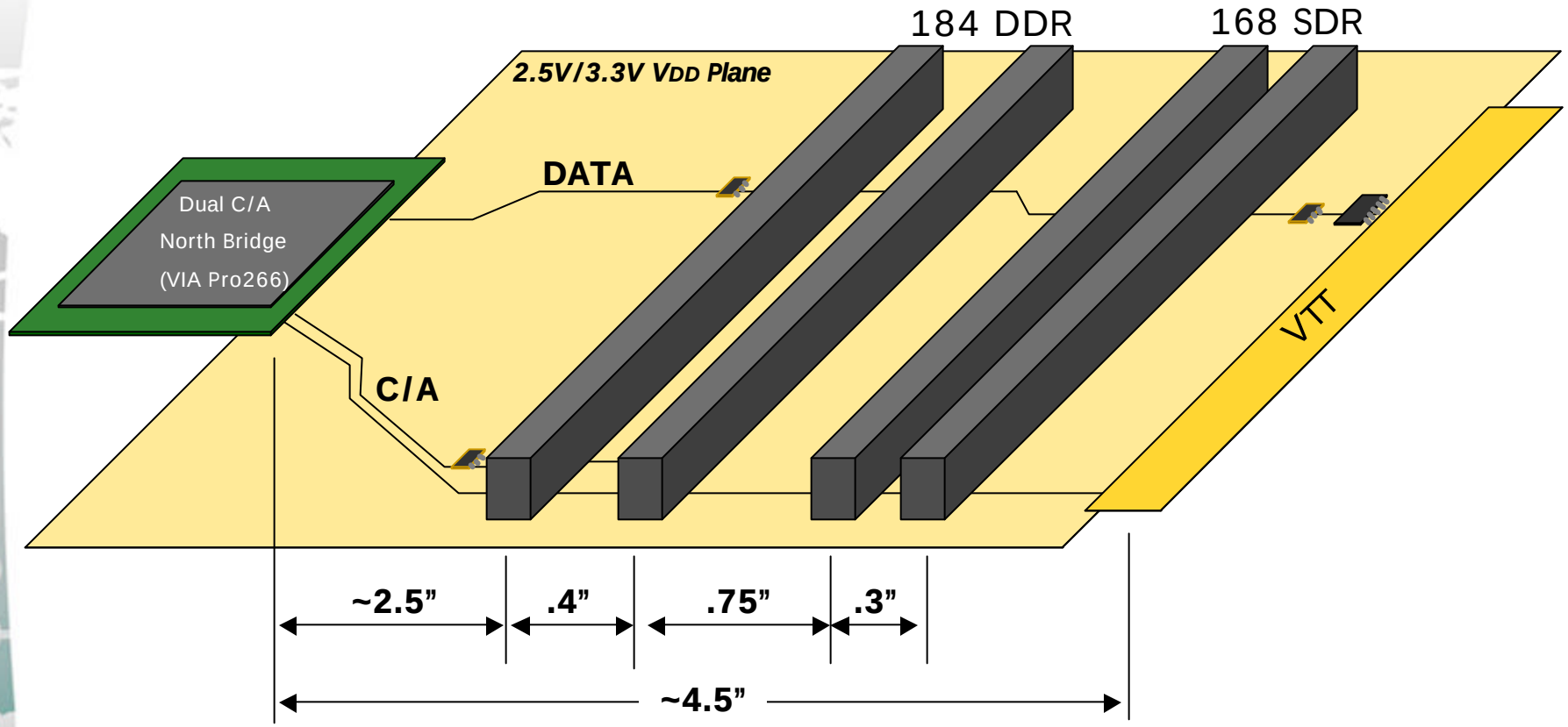
1 Copy, 2 Unbuffered DIMMs



- Address lines interact on common bus to create ISI (reflection) timing push out
- Many systems eliminate RT to save cost
- Data lines typically are not a problem

Mixed DDR/SDR System

One of Many Examples



2T addressing - OK

Data load limited to 2 DIMMs at a time

Desktop Implementations

- Type A, PC2100
  - 2-copy C/A, 3 Unbuffered DIMMs, 2T per command
- Type B, PC2100
  - 1-copy C/A, 2 Unbuffered DIMMs, 2T per command
  - Even some trying 3 here, with some success
- Type C, PC2100
  - 2-copy C/A, 2 Unbuffered DIMMs, 1T per command
- Ultimate goal, PC2700
  - 1-copy C/A, 2 Unbuffered DIMM, 1T per command

Server

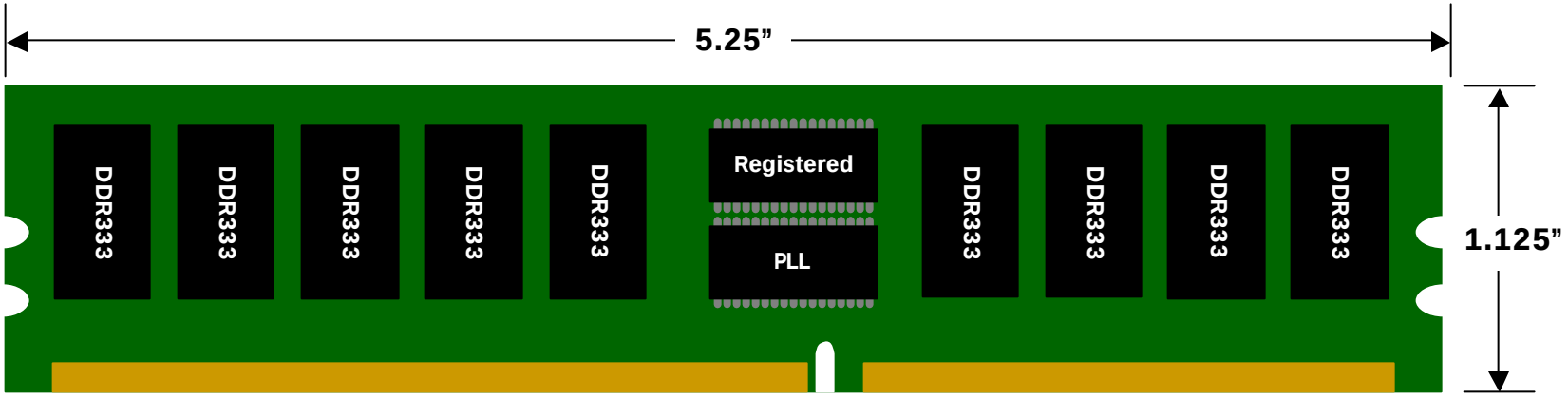
- Traditional chassis with 1.7” Registered DIMMs
- 1U interest is very high
  - Reduced-height Registered DIMM is being addressed by standards groups; JEDEC, JEITA
  - Micron is in development of a 1.125” Registered DIMM for PC1600 and PC2100 systems
    - FBGA packaging for SDRAM
    - Meets all electrical characteristics of common TSOP-based common Gerber
    - 256MB and 512MB samples 2Q01; production 3Q01
    - Evolutionary to PC2700 Registered DIMM

Server

- 4 DIMM/channel, PC1600
  - Standard termination, series-R and parallel to VTT
  - Systems running very stable at this speed
- 4 DIMM/channel
  - Two possibilities
    - 2-copy C/A, 2 Registered DIMMs per copy, 1T command
      - Standard termination
      - High-performance, flip-chip BGA for ASIC
    - 1-copy C/A
      - Requires new termination: capacitive-compensated
      - Standard, wire-bond BGA package

Low-Profile Registered DIMM

- FBGA SDRAM package, JEDEC registration
- Designed to match TSOP-based module topology and timing as closely as possible



- Provides a 90° (no angled sockets) solution for 1U servers

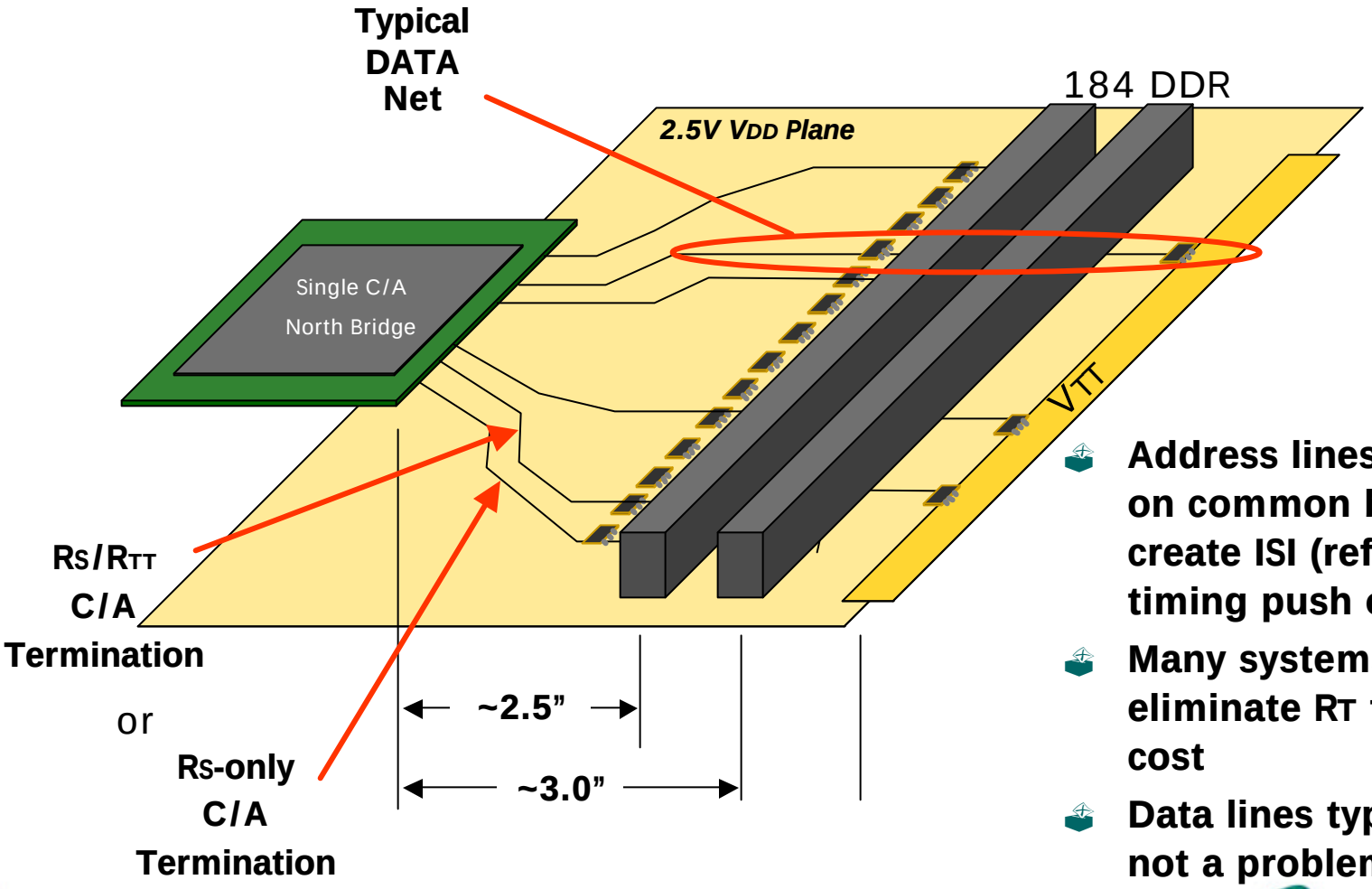
Notebook

- DDR SODIMMs are available
  - Common Gerbers are done and production ready
- DDR has a big power advantage over PC133
  - Current system benchmarks showing approximately 30% lower power than PC133
  - This at the 2X bandwidth of DDR266/PC2100!
- Mechanical design very similar to SDR
  - Most systems can be designed without major changes to cases

Second Generation DDR Design

Example of Typical DDR Channel

1 Copy, 2 Unbuffered DIMMs

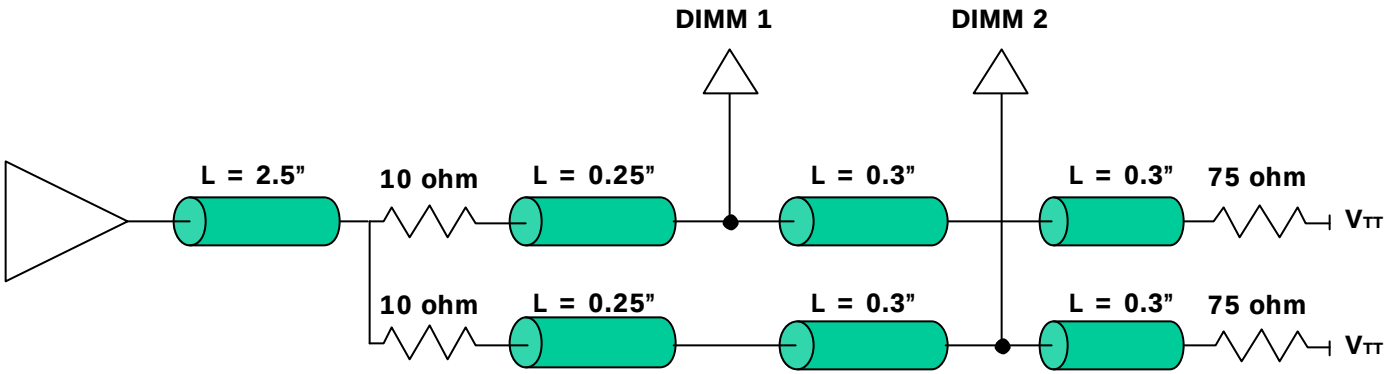


- Address lines interact on common bus to create ISI (reflection) timing push out
- Many systems eliminate RT to save cost
- Data lines typically are not a problem

Getting More Bandwidth

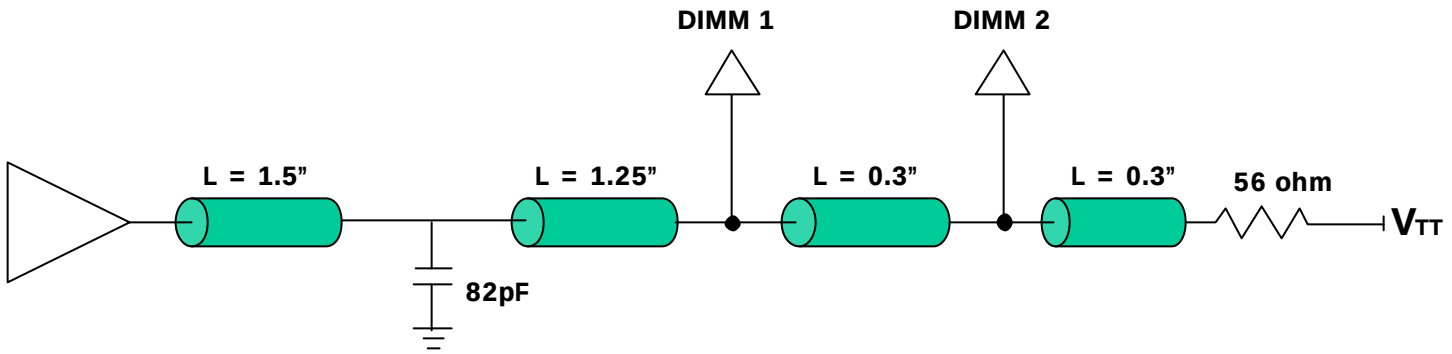
- Techniques for better margin, little added cost
  - Improved termination schemes for motherboard
  - Active termination in chipset
- Improved interoperability due to increases in system margin at high frequency, mixed loads
- Provides a “spring board” to move motherboard designs to PC2700

Split-Bus Termination for Command/Address Bus



- Example C/A route
- Splitting bus isolates the DIMM loads from one another
- I/O power reduced over standard termination by using high value RTT
- No changes to ASIC driver necessary to see improvements
- Works with all DDR DIMM common Gerbers

Capacitive Compensation Termination for Command/Address Bus

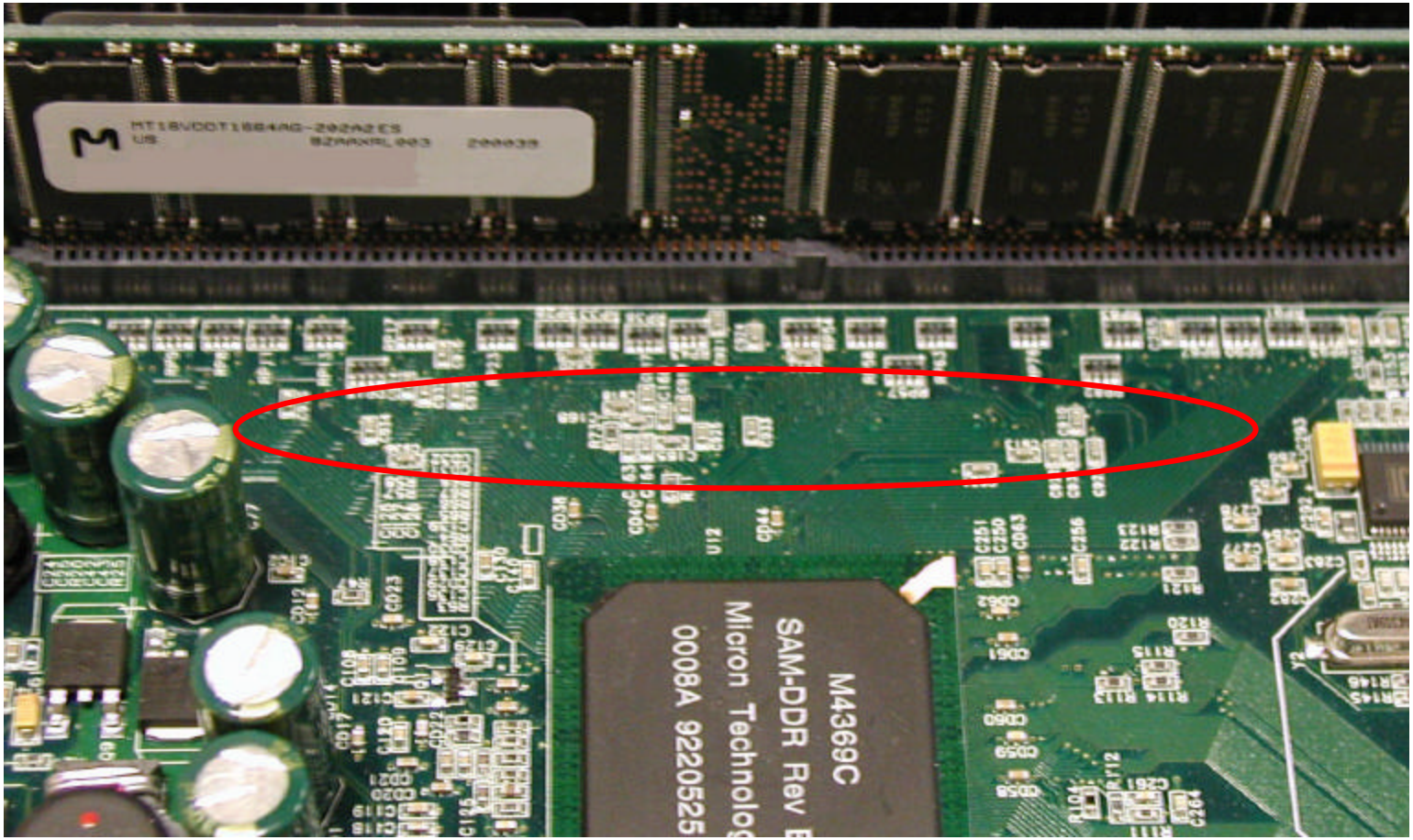


- Example C/A route
- Capacitor tunes frequency response of channel to limit ISI/reflections
- Some added propagation delay added due to R/C
- No changes to ASIC driver necessary to see improvements
- Works with all DDR DIMM common Gerbers

Micron Hurricane Board

With Compensated C/A Net

- **Capacitive compensation of 82pF on Command/Address**



Correlating Systems to Simulation

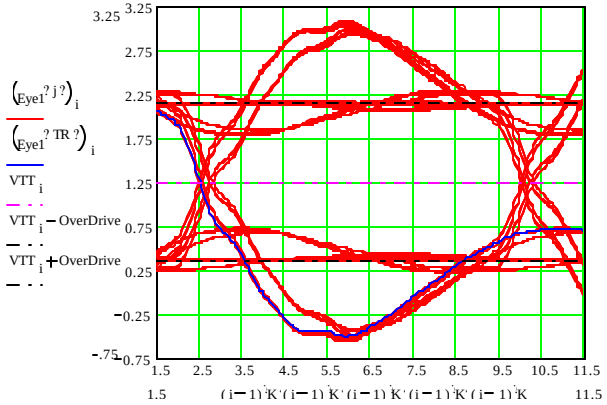
1st Slot: 4 Devices, 2nd Slot: None (Monitoring 1st Slot)

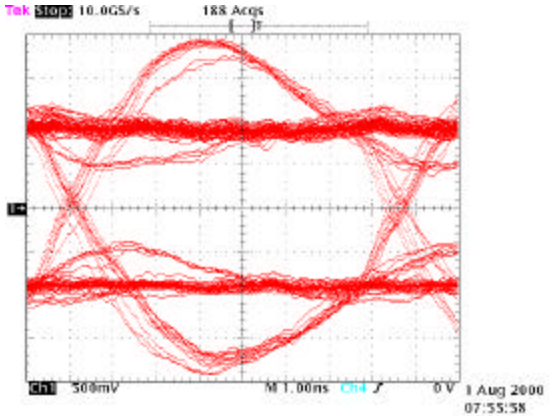
(Note: Scale change from non-compensated to compensated)

Simulation

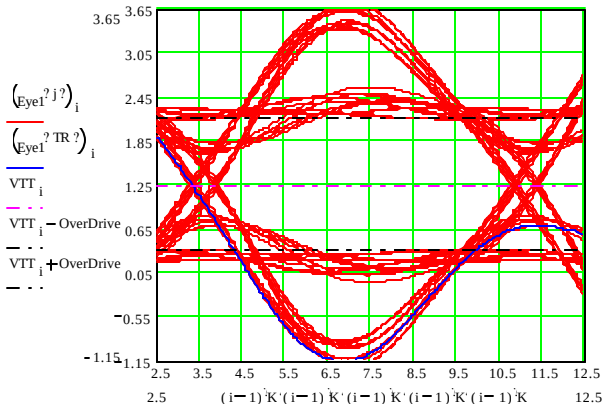
Hardware Measurement

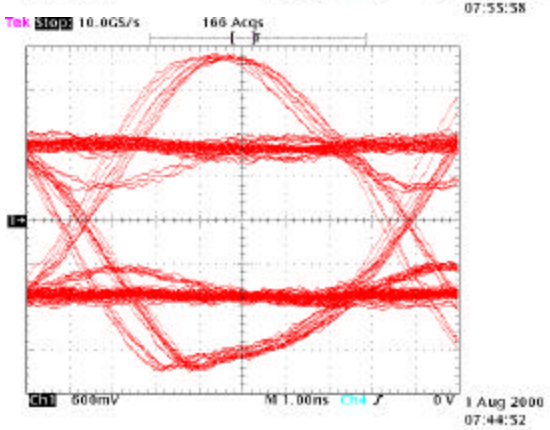
Non-Compensated
Rs = 10 ohms
Fcap = none





Compensated
Rs = none
Fcap = 82pF





- **The modeling technology used by Micron has excellent correlation to actual systems**

Command/Address Loading

- **Command rates possible at PC2100/DDR266**

C/A Bus	*R_S*	*R_S/R_{TT}*	*R_{TT}*	*C/R_{TT}*	*$2xR_S/R_{TT}$*
1 Copy, 2 DIMM	2T	2T	2T	1T	1T
2 Copy, 2 DIMM	1T	1T	1T	1T	N/A

Worst-Case Corner at PC2100

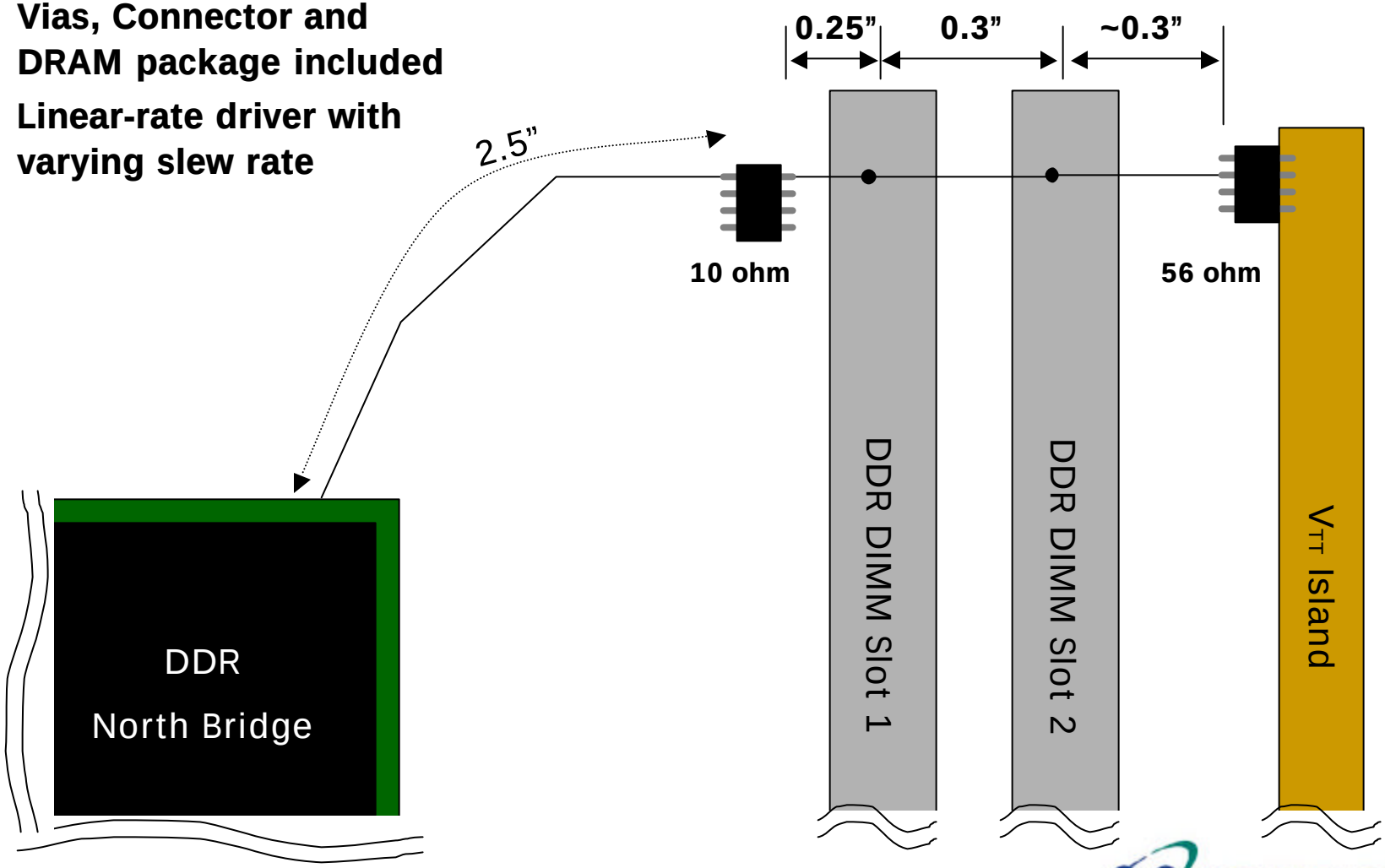
- 2 Unbuffered DIMMs, single-copy C/A system
  - Mixing DIMM loads can create reflection/ISI noise on edges of Command/Address
    - Light-load, 4-component DIMM in front slot; heavy-load, 16-component DIMM in the second slot
    - ASIC driver will affect the impact of module loading as well
  - Some only running with RS for termination on C/A
- Data net is much better balanced
    - Modules are only 1 or 2 loads per slot

PC2100 Command Rate Targets

- Today all single-copy C/A systems are running 2T command rate (clocks per command)
  - Systems with only RS will only run here
- The goal
  - Embedded Northbridges (3D on-board) want to run 1T command rate, with a single C/A copy
  - Termination and board layout must be improved to accomplish this
  - Limit cost adders, but can't avoid some added cost

Simulation of Mixed DIMM

- Vias, Connector and DRAM package included
- Linear-rate driver with varying slew rate



Simulation of Mixed DIMM

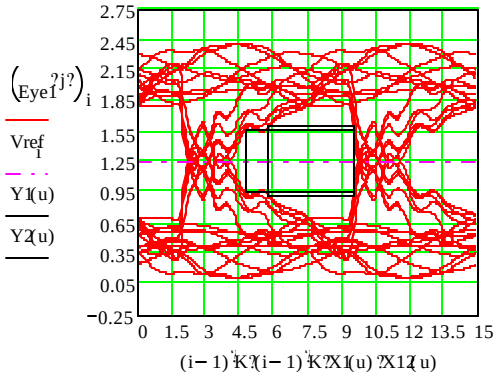
Input Slew Rate ~ 5V/ns
Slot 1 - 5 Devices, Slot 2 - 18 Devices

ISI_0 ? 2?10^3 psec

$Apert2_0$? 3.697nsec

$SlewR_0$? 0.24V/nsec

Slot 1

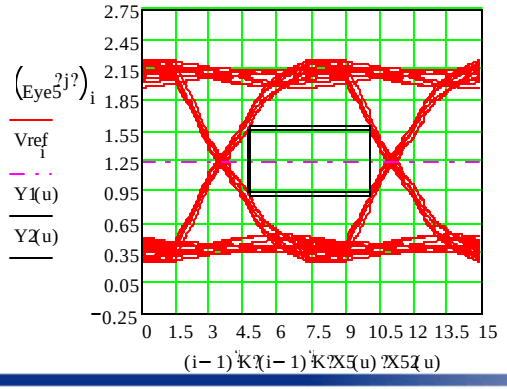


ISI_4 ? 435psec

$Apert2_4$? 5.253nsec

$SlewR_4$? 0.31V/nsec

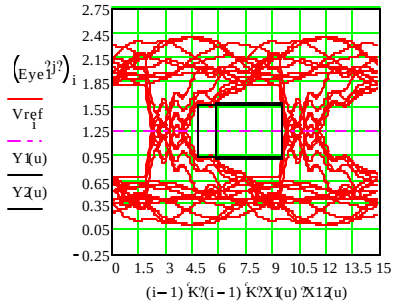
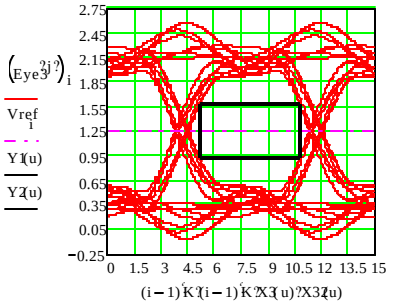
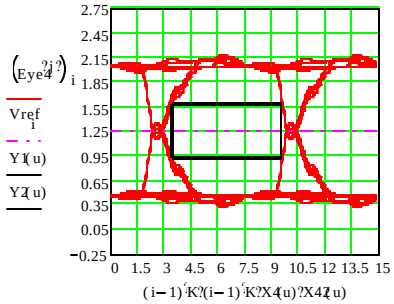
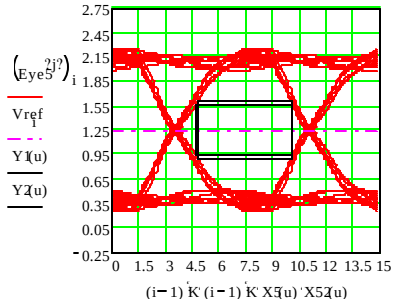
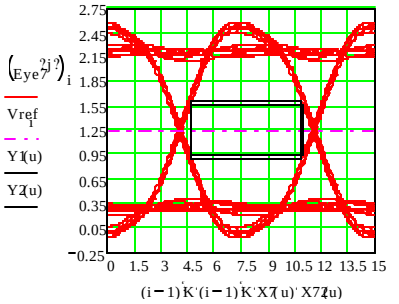
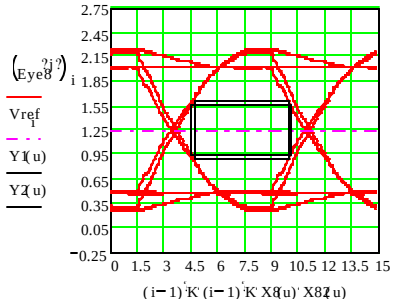
Slot 2



- Standard termination
- First DIMM shows eye reduction due to ISI
- Topology mismatch between two DIMMs creates reduction
- Second DIMM has well-defined eye
- Worst case for this topology

Improved-Performance Scenarios

Input Slew Rate ~ 5V/ns
Slot 1 - 5 Devices, Slot 2 - 18 Devices

	Standard		Compensated	Split Bus
Slot 1	ISI$_0$? 2?10^3 psec Apert2$_0$? 3.697nsec SlewR$_0$? 0.24V/nsec		ISI$_2$? 790psec Apert2$_2$? 5.488nsec SlewR$_2$? 0.49V/nsec		ISI$_3$? 573psec Apert2$_3$? 6.133nsec SlewR$_3$? 0.50V/nsec	
Slot 2	ISI$_4$? 435psec Apert2$_4$? 5.253nsec SlewR$_4$? 0.31V/nsec		ISI$_6$? 234psec Apert2$_6$? 6.146nsec SlewR$_6$? 0.60V/nsec		ISI$_7$? 287psec Apert2$_7$? 5.328nsec SlewR$_7$? 0.34V/nsec	

Improvements to eye aperture and voltage level

Large reduction in noise component

Improvements to eye aperture and voltage level

Improved-Performance Scenarios

Input Slew Rate ~ 5V/ns

Slot 1 - 18 Devices, Slot 2 - 18 Devices

	Standard		Compensated	Split Bus
Slot 1	ISL$_0$? 226psec Apert2$_0$? 4.435nsec SlewR$_0$? 0.24V/nsec	**Improvements to eye aperture and voltage level**	ISL$_2$? 358psec Apert2$_2$? 5.695nsec SlewR$_2$? 0.44V/nsec	ISL$_3$? 637psec Apert2$_3$? 5.159nsec SlewR$_3$? 0.34V/nsec
Slot 2	ISL$_4$? 125psec Apert2$_4$? 4.857nsec SlewR$_4$? 0.26V/nsec	**Improvements to eye aperture and voltage level**	ISL$_6$? 214psec Apert2$_6$? 5.912nsec SlewR$_6$? 0.50V/nsec	ISL$_7$? 569psec Apert2$_7$? 5.155nsec SlewR$_7$? 0.32V/nsec

Worst-Case Scenarios

Bus Type	ISI (ps)	Loading	APT2 (ns)	Loading	Min Amp (V)	Loading
Standard	1880	(5,18)	3.664	(5,18)	-0.261	(5,0)
Standard with 10 stub on 5 device	1110	(5,18)	3.774	(5,18)	0.44	(5,0)
Compensated with 10 stub on 5 device	789	(5,18)	5.473	(5,18)	-0.078	(5,18)
Split bus	637	(18,18)	5.125	(18,18)	-0.134	(5,0)
Split bus with 10 stub on 5 device	637	(18,18)	5.125	(18,18)	0.138	(5,0)

ISI = Timing skew due to Inter-symbol interference

APT2 = Data eye time at ±350ps from V_{REF}

Min Amp = Undershoot voltage amplitude (overshoot)

Loading = Module load condition of worst case measurement

Design Impact

- Compensated Bus
  - Replace RS with capacitor
  - Systems that only use RS must add RT
  - Chip-capacitors best solution and lower cost than C-pack for C/A
  - 18 caps and 5 R-packs
    - Adds about $0.14 US
  - Adds 500ps - 1ns of propagation delay to C/A signals
- Split Bus
  - 18 additional lines to terminate
  - 9 additional R-packs for RS and RT
    - Adds about $0.09 US
  - No change in propagation delay

Conclusions

- **Compensated scheme and Split Bus provide dramatic improvements in timing and signal integrity**
  - **Both are very cost effective solutions for high performance memory**
  - **No added cost for motherboard, just a little extra layout time**

Improving Read Data Eye Margin

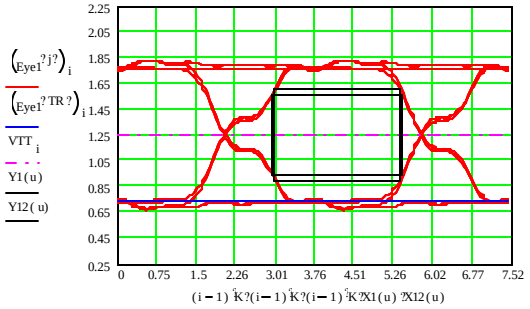
Active Termination in Northbridge

Standard Termination

Slew Rate ~ 3.6 V/ns

OverDrive1 ? 0.310 V
Aperature1 ? 2.500 nsec
SlewRate1 ? 0.48 V/ nsec

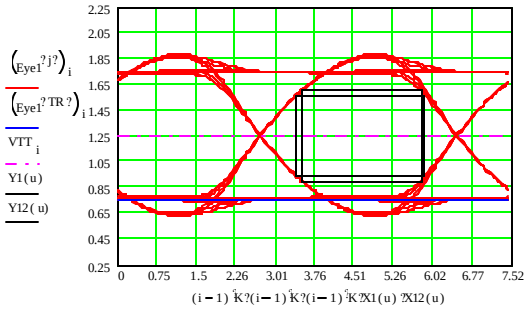
OverDrive2 ? 0.350 V
Aperature12 ? 2.417 nsec



Compensated With Active Termination

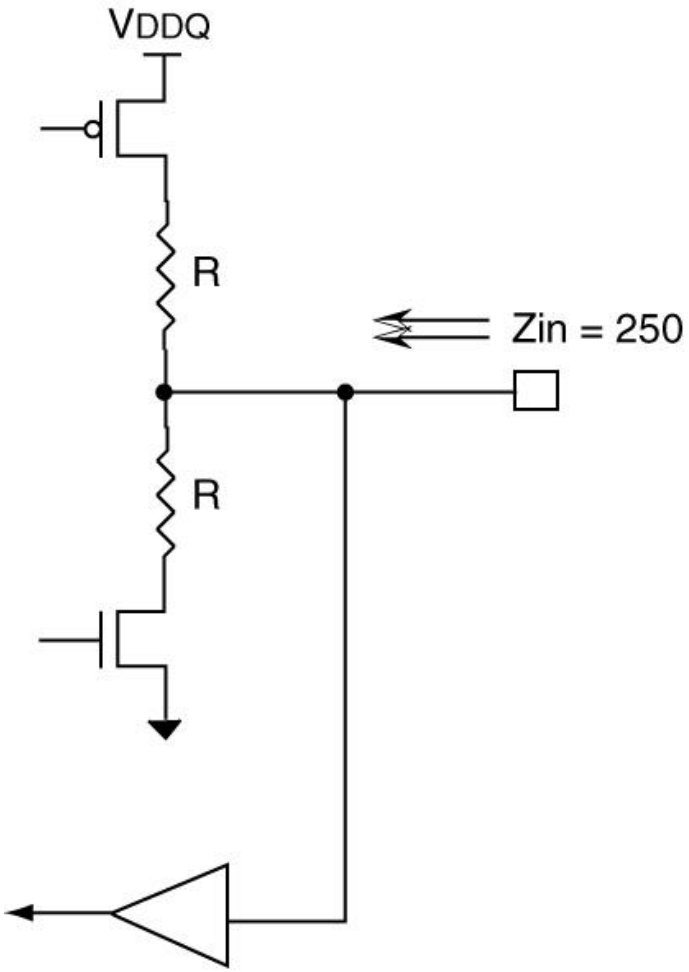
OverDrive1 ? 0.310 V
Aperature1 ? 2.458 nsec
SlewRate1 ? 0.47 V/ nsec

OverDrive2 ? 0.350 V
Aperature12 ? 2.250 nsec



- Even with new termination, reads can benefit from improved system margins
- Provides robust system for PC2700 modules
- Adds little cost, if any, to ASIC

Active Termination Implementation



- Input impedance of about 250 ohms works well
  - Signal integrity is not highly sensitive to the absolute value
- FETs on the far side of the resistors (from the pad) will reduce effective input capacitance
- Especially beneficial in 3 and 4-DIMM systems

DDR Migration to PC2700

PC2700

- Unbuffered system requirements
  - 1T command rate must be supported
  - Two assumptions
    - 2 C/A copy, 1T, 2 Unbuffered DIMMs, options for termination
    - 1 C/A copy, 1T, 2 Unbuffered DIMMs, new termination
  - Support for TSOP and FBGA packages
  - Component must be speed sort of current SDRAM designs
    - Keep costs down

PC2700 Modules

- **Unbuffered**
  - **FBGA-based can be as low at 1” height**
- **Registered**
  - **1.125” max height**
  - **FBGA-based only, no stacking**
- **SODIMM**
  - **Could be TSOP or FBGA**
- **MicroDIMM**
  - **Most likely to be FBGA-based**

PC2700 Schedule

- Prototype/samples of standard
  - 3Q01 - 256Mb
- Validation and qual
  - 3Q01 - 256Mb
- Production
  - 1Q01 seen as the required need
- Price of PC2700 = PC2100?
  - 2H02 estimated

Summary

- DDR standard updates
  - New SPDs
- Necessity of mixed DDR/SDR systems
  - Good way to transition, but be careful
- New termination schemes to increase performance
  - Big gains in timing/noise margin, little added cost
- Proposal to improved read data capture
  - Easy addition to chipset driver to improve reads
- PC2700 development will be complete this year